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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,471	09/22/2003	Fumihiko Kato	03FN021US	5531

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EXAMINER	
LUI, DONNA V	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,471	KATO, FUMIHIKO	
	Examiner	Art Unit	
	Donna V. Lui	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/03, 11/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. **Claims 1, 3, and 5** are objected to because of the following informalities: The following claims were interpreted as follows. Appropriate correction is required.

Claim 1, page 18, line 8: first high-potential ~~low-potential~~ power supply and a voltage of said first

Claim 3, page 19, line 20: terminals that constitute ~~constituting~~ the associated reference-voltage

Claim 3, page 19, line 23: terminal group, the ~~that~~ reference-voltage output terminal which

Claim 3, page 19, line 27: an operational amplifier having a positive input ~~output~~

Claim 3, page 20, line 2: selector is input, a negative input ~~output~~ terminal connected to

Claim 5, page 20, line 14: plurality of switches having ~~one~~ ends connected together to

Claim 5, page 20, line 18: enables the ~~that one of said~~ switches which are ~~is~~ selected based on

Claim 6, page 20, line 23: switches having ~~one~~ ends connected together to said first

Claim 6, page 21, line 3: said first switch circuit and having ~~one~~ ends connected

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-5, and 7-11** are rejected under 35 U.S.C. 102(e) as being anticipated by Kudo et al. (US 2002/0186230 A1).

With respect to **Claim 1**, Kudo discloses a gamma correcting circuit *(See figure 3)*. Kudo teaches the circuit to comprise a basic voltage generating circuit *(See figure 3, 307)* which has one end connected to a first high-potential power supply *(316)* and the other end connected to a first low-potential power supply *(GND)* and generates and outputs a plurality of basic voltages by dividing a voltage difference between a voltage of the first high-potential power supply and a voltage of the first low-potential power supply *(page 4, [0047], lines 5-10)*; a gamma correction resistor circuit *(315)* having a plurality of resistor elements connected in series between a second high-potential power supply *(output of the first amplifier of 314; the second high-potential power supply is a derivation of the first high-potential power supply)* and a second low-potential power supply *(output of the last amplifier of 314; the second low-potential power supply is a derivation of the first low-potential power supply)*, and gray-scale voltage output terminals *(terminals to the right of 315)* and n reference-voltage output terminal groups *(outputs of selector circuits SEL 308-313)*, both provided at respective nodes between the resistor elements, each of the n reference-voltage output terminal groups including a maximum of u *(outputs of selector circuits SEL 308-313; note that n=u)* reference-voltage output terminal candidates; and a gamma correction adjusting circuit *(selector circuits 308-313)* having n gamma characteristic adjusting units *(figure 7A, 701: denotes one of the selector circuits)* in association with the n reference-voltage output terminal groups *(selection of 706 is inputted to the amplifier circuit)*, each of

which selects one of a maximum v basic voltages *(figure 3, terminals to the left of the selector circuits SEL)* supplied from the basic voltage generating circuit as a reference voltage based on correction adjustment data *(306; page 4, [0047], lines 8-11)* and selects an output terminal for the selected reference voltage from the maximum of u reference-voltage output terminal candidates included in the associated one of the n reference-voltage output terminal groups based on the correction adjustment data *(depending on the switch configuration shown in figure 7A, only one reference voltage is selected for an output terminal)*.

With respect to **Claim 2**, Kudo teaches the basic voltage generating circuit *(See figure 3, 307)* has a plurality of resistor elements connected in series between the first high-potential power supply *(316)* and the first low-potential power supply *(GND)* and outputs individual basic voltages from nodes between those resistor elements *(equivalent to inputs of the selector circuits SEL)*.

With respect to **Claim 3**, Kudo teaches the gamma characteristic adjusting units to include a data latch which fetches and latches the correction adjustment data at a predetermined timing *(page 9, [0085], last seven lines; the correction adjustment data is equivalent to data written to the micro adjustment register 306)*; a reference voltage selector *(See figure 7A, 704)* which receives a plurality of basic voltages and selects and outputs one of the basic voltages as a reference voltage based on the correction adjustment data latched by the data latch *(page 7, [0075], last five lines; data from 703)*; a node selector which has a first terminal *(See figure 3, outputs of the amplifiers 314)*, a second terminal *(outputs of the amplifiers 314, note that the first*

terminal is equivalent to the second terminal), a switch circuit *(303: decoder)* and a plurality of voltage output terminals *(outputs from the decoder circuit)* that constitute the associated reference-voltage output terminal group and selects, from the voltage output terminals of the associated reference-voltage output terminal group, the reference-voltage output terminal *(input to 314)* which is connected to the first terminal and the second terminal by the switch circuit *(303)*, based on the correction adjustment data latched by the data latch *(306)*. Kudo teaches an operational amplifier *(314)* having a positive input terminal to which an output of the reference voltage selector is input *(output from the selector circuit is input to 314)*, a negative input terminal connected to the first terminal *(the first terminal being the output of the operational amplifier)* and an output terminal connected to the second terminal *(the second terminal being the output of the operational amplifier that connects to 315; note that the first terminal is equivalent to the second terminal)*.

With respect to **Claim 4**, Kudo teaches the reference voltage selector to select a reference voltage based on a first predetermined portion *(See figure 7A, due to the [0] bit of 703)* of the correction adjustment data latched by the data latch and the node selector selects a reference-voltage output terminal based on a second predetermined portion *(due to [2] bit of 703)* of the correction adjustment data *(note that the predetermined portions are based on each bit of the correction adjustment data)*.

With respect to **Claim 5**, Kudo teaches the switch circuit *(See figure 3, 303)* of the node selector includes a plurality of switches *(note that a decoder is comprised of a plurality of*

transistors which are also switches) having ends connected together to the first terminal and the second terminal *(since the first and second terminals are equivalent, then the terminals (inputs to the decoder) are connected to one end of the switch, "decoder")* and other ends *(output of the decoder)* connected to respective voltage output terminals of the associated reference-voltage output terminal group and enables the switches which are selected based on the correction adjustment data *(See figure 7A, 703; note that 703 outputs correction adjustment data for controlling the switches 704, 705, and 706 and therefore influence the output of the voltage from the node selector).*

With respect to **Claims 7-11**, Kudo teaches a display panel drive apparatus having a gamma correcting circuit *(page 1, [0001])*.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 6 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudo as applied to claim 1 above, and further in view of Kajihara et al. (Pub. No.: US 2002/0050970 A1).

With respect to **Claim 6**, Kudo does not teach a node selector that has: a first switch circuit including a plurality of switches having ends connected together to the first terminal and

other ends connected to respective voltage output terminals of the associated reference-voltage output terminal group; and a second switch circuit including a plurality of switches provided in association with the switches of the first switch circuit, equal in number to the switches of the first switch circuit and having ends connected together to the second terminal and other ends respectively connected to the other ends of the switches of the first switch circuit, and enables that one of the switches of the first switch circuit which is selected based on the correction adjustment data and that one of the switches of the second switch circuit which is associated with the selected switch.

Kajihara teaches a node selector that has: a first switch circuit *(See figure 4, 109-116)* including a plurality of switches having ends connected together to the first terminal *(the first terminal is the output of the voltage follower with differential amplifier 126 (page 10, [0144], lines 4-6))* and other ends connected to respective voltage output terminals of the associated reference-voltage output terminal group *(terminal leading to the DA converter)*; and a second switch circuit *(117-124)* including a plurality of switches provided in association with the switches of the first switch circuit *(provided in association is equivalent to sharing the same output terminal to the DA converter)*, equal in number to the switches of the first switch circuit and having ends connected together to the second terminal *(having ends connected together to the second terminal is equivalent to the path through elements 101 to 108 corresponding to 117-124 and 109-116 when switched on, and to the input terminal of the 126)* and other ends respectively connected to the other ends of the switches of the first switch circuit, and enables that one of the switches of the first switch circuit which is selected based on the correction adjustment data and that one of the switches of the second switch circuit which is associated with

the selected switch *(the correction adjustment data is equivalent to SW, page 9, [0140] and [0141], lines 1-6; the first switch circuit is enabled by the SW signal from the analog switch control circuit section 40 and the switches of the second switch circuit operate in association with the selected switch. Operation of the switches can be seen from the waveform of figure 5).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the node selector of Kajihara to the gamma correcting circuit of Kudo for the purpose of having tone display voltages outputted via the buffer *(voltage follower with amplifier)* with a low output impedance, only when a large charge or discharge current is required for the pixel capacitors of the liquid crystal panel or for the wire capacitors of the source signal lines, so as to attain spontaneous rise and fall of the tone display voltages whereas the tone display voltages drawn from the reference voltage generator are directly outputted without utilizing the buffer when in a steady state and no such large current is required, such as a time when a high output impedance state does not pose any problem *(page 12, [0173])*.

With respect to **Claim 12**, Kudo teaches a display panel drive apparatus having a gamma correcting circuit *(page 1, [0001])*.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donna V Lui
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PRIMARY EXAMINER